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DESIGN AND EVALUATION OF A LOW-VOLTAGE PROCESS VARIATION-TOLERANT SRAM

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ABSTRACT: present three iterations of SRAM bit cells with nMOS-only based read ports aimed to greatly reduce data dependent read port leakage to enable 1k cells/RBL, improve read performance, and reduce area and power over conventional and 10T cell-based works. We compare the proposed work with other works by recording metrics from the simulation of a 128-kb SRAM constructed with divided-word line-decoding architecture and a 32-bit word size. Apart from large improvements observed over conventional cells, up to 100-mV improvement in read-access performance, up to 19.8% saving in energy per access, and up to 19.5% saving in the area are also observed over other 10T cells, thereby enlarging the design and application gamut for memory designers in low-power sensors and battery-enabled devices. As an enhancement of this concept, 11T SRAM single ended Schmitt trigger is proposed to reduce area and power. A Schmitt-trigger-based single-ended 11T SRAM cell, which significantly improves static noise margin (SNM) and consumes low power leakage power dissipation is also main advantage with this enhancement The proposed cell significantly improves HSNM and RSNM while consuming least energy per operation among all the considered cells.
Keywords: Static Random Access Memory, static noise margin, PROCESS VARIATION

INTRODUCTION: By the analysis of Schmitt-Trigger (ST)- based differential- sensing static random access memory (SRAM) bit cells for ultralow-voltage operation, the ST-based SRAM bit cells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The proposed ST bit cells incorporate a built-in feedback mechanism, achieving process variation tolerance which is a must for future nanoscaled technology nodes. A detailed comparison of different bit cells shows that the ST-1 , ST-2 and proposed bit cell can operate at lower supply voltages. POrtable electronic devices have extremely low power requirement to maximize the battery lifetime. Variousdevice-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations.Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, writefailure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories,

which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2]. In a given process technology, the maximum supply voltage (referred to as Vmax) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits.Vmax is reducing with the technology scaling due to scaling of gateoxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as Vmin), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, is increasing, and this closes the gap between Vmax and Vmin[5]. Hence, to enable SRAM bit cell operation across a wide voltage range, Vmin has to be further lowered. Various design solutions such as read-write assist techniques and bit cell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bit lines, bit cell VSS node, and bit cell VCC node). In this case, SRAM Vmin can be lowered without adding extra transistors to the six–transistor (6T) bit cell. Various bit cell topologies are also proposed to enable low-voltage operation. In this work, focus will be only on various bit cell configurations.

LITERATURE SURVEY: NVSRAM is one of the advanced NVRAM technology that is fast replacing the Battery-backed SRAMs that need battery free solutions and long term retention at SRAM speeds. For instant on-off operation better non volatile performance is essential [1].Better SRAM performance in terms of leakage power , access time ,robustness is essential [2].The average power dissipiation should be less [3].The 8T SRAM cell as compared to conventional 6T SRAM cell achieved improved read stability, read current and leakage current [4]. Write power i.e. power dissipiation in SRAM should be less [5]. The issue associated with transistor scaling and power management are addressed [8].The operating voltage for cell should be minimum [6]. The inverters are optimized for high noise margin[7] The use of SRAM is expected to increase in future for both portable and high performance microprocessor. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, and portable multimedia devices [1]. To achieve higher speed microprocessor, SRAM based cache memories are commonly used. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability [2]. Nowadays research on very low threshold voltage and ultra-thin gate oxide are in progressive stage, due to reduction in the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness further degrade the stability of SRAM cells [3-5]. Jaydeep P. Kulkarni [1]. The proposed shows ultra-voltage operation of different SRAM cell is explained The ultra-voltage operation is performed by lowering the supply voltage. The proposed ST-2-bit cell gives 1.6 times higher read static margin and 2 times write static margin as compare to 6T SRAM. For achieving low voltage operation 6T/8T/10T/ST SRAM topologies are studied in this paper. Results are carried out at 130nm technology, which give the effectiveness of proposed bit cell for successive ultra-low voltage operation. Mohsen Imani, HalehAlimohamadi [2] proposed low power 12T SRAM cell with 16nm at 800mv supply voltage CMOS technology. The proposed 12T SRAM cell is compared with the 9T and 10T SRAM cell which shows that the leakage current is reduced by using two stack transistors at read path. The reliability of cell also increases by increasing read SNM. The proposed cell has 5.5% and 27.4% higher read SNM from 9T and 10T respectively. The power consumption of proposed 12T cell has lowered by 35.5% and 43.8% as comparison of 9T cell and 10T cell. Ambrish Mall, SuryabhanPratap Singh, Manish Mishra, GeetikaShrivastava[3], states that this paper gives the brief development in low power circuit. In standby mode the power consumption is more. The proposed circuit contains a series connected tail transistor which turn down the leakage current which results in, low power consumption of cell. The proposed 12T SRAM cell is compared with low power 10T SRAM cell on 45nm and 32nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) respectively.

EXISTING ARCHITECTURE:

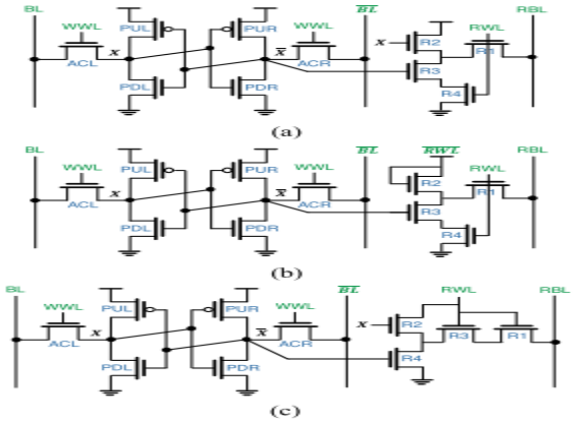

Fig. 1. Schematic of the proposed (a) 10T-P1 (b) 10T-P3 (c) 10T-P2 cells.

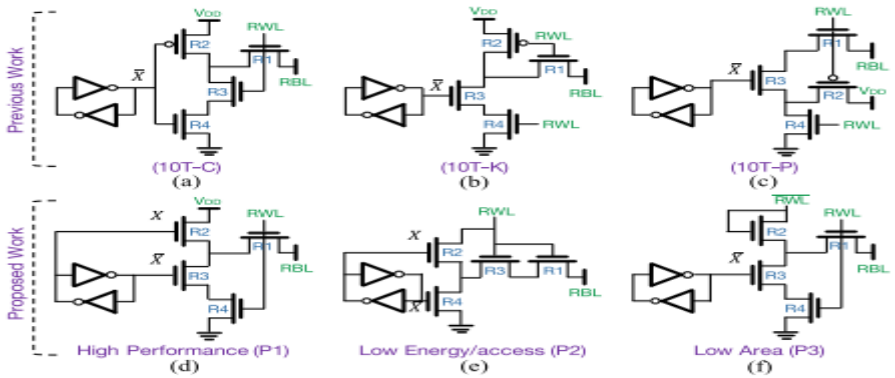

Fig. 2. Schematic of the proposed cell internal

TOPOLOGY OF PROPOSED BIT CELLS:

The schematic of the proposed 10T SRAM cells is shown in Fig. 2. Each of them comprises of cross coupled inverters (PUL-PDL and PUR-PDR) and two access transistors (ACL and ACR). The read port of each cell consists of four nMOS (R1, R2, R3 and R4). The read port in Fig. 2(a) has improved data-dependent read bit-line leakage and is aimed at high performance. The read ports in Fig. 2(b) and (c) have complete data-independent read bit-line leakage and are aimed at very low power and high density respectively. From here on, the proposed cells are referred to as 10T-P1, 10T-P2 and 10T-P3.

BIT CELL WORKING MECHANISM: When operating in near and sub-threshold region, the ION/IOFF is severely degraded and it becomes increasingly difficult to implement greater number of cells on a single column. As the number of cells increase, the combined passgate leakage becomes comparable to the read current, thereby making it difficult for the sense amplifier to correctly evaluate the read bit-line voltage level. Furthermore, the data stored in the cell also affects the read bit-line leakage, thereby making the off-state read bit-line leakage current to fluctuate highly. This is exacerbated at ultra-low voltages, where the worst-case data pattern can lead to the RBL voltage level of 'zero' becoming greater than the RBL voltage level of 'one' [29]. In order to improve the ION/IOFF ratio, the read port shown in Fig. 3(a) was proposed in [1]. When the cell stores 'one,' the R2 pMOS charges the intermediate node, thereby greatly reducing the read bit-line leakage through R1 nMOS. However, this also leads to flow of leakage current from intermediate node into the RBL. The combined leakage of all cells on the same column can raise the low logic level of RBL to several hundred millivolts, thereby leading to reduced voltage swing and sensing margin. The conceptual scenario of the effective read bit-line voltage swing for this case has been depicted in Fig. 4(a). On the other hand, when the cell stores 'zero,' the RBL leakage is reduced through the stacking effect of nMOS. Therefore, such a topology

makes the effective RBL swing largely dependent on the data pattern in the column. In another work [3], the data dependency was removed by creating a data-independent leakage path between the cell's read port and the RBL. This led to a significant voltage swing on the RBL even at lower voltages. The read port and the corresponding effective RBL swing for the same has been shown in Fig. 3(b) and Fig. 4(b) respectively. A recent work [2], also proposed a modified read port [shown in Fig. 3.(c)], to improve the ION/IOFF ratio. However, it is also

READ AND WRITE CAPABILITY ANALYSIS: Assuming that the stored value of the RHPD-12T memory cell is set as digital logic "1," that is, Q= "1," QB="0," S1="1," and S0= "0." The read and write operations of the RHPD-12T circuit are analyzed in detail as follows. In the process of reading operation, after the precharge stage, the voltages of the two bit lines are increased to high voltage "1." When WL is in high voltage (WL= "1"), four access nMOS transistors are turned ON, for read operation, the four internal storage nodes for keeping the stored data. The voltage of BL retains the value "1," but the voltage of BLN is decreased due to the discharge through N3 and N6. When the voltage difference between BL and BLN is obtained, which will be detected by the differential sense amplifier present in the circuit, the data stored in the memory cell will be the output. For the write operation, it is assumed that data "1" is written to the proposed RHPD-12T cell, the bit lines BL and BLN need to be "1" and "0," respectively. When the voltage of WL is high, the write operation is executed. Transistors N1, N3, and N6 are turned ON, P1 is OFF, at that moment, and the Q node data is stored as "1," indicating that data "1" can be successfully written into the proposed RHPD-12T memory cell. In Semiconductor Manufacturing International Corporation (SMIC) CMOS 65-nm technology, the timing simulation of the proposed RHPD-12T memory cell has been carried out, and the corresponding results are shown in Fig. 2. From Fig. 2(a), "write 0, read 0, write 1, read 1" transient simulation results indicated that the proposed RHPD-12T cell can execute the write and read operations successfully. Writing capability is another important factor in measuring the basic performance of the memory cells.

PROPOSED TECHNIQUE:

SCHMITT-TRIGGER-BASED SRAM CELL DESIGN:

The stability of cross-coupled inverter pair in SRAM cell operating at very low supply voltage is not very promising. Furthermore, power consumption is high due to degraded inverter characteristic. Therefore, an ST inverter is used to exploit the improved inverter characteristic. The basic element for the data storage in an ST-based SRAM cell uses a crosscoupled ST-based inverter pair shown in Fig. 1(a) [22]. ST is like a comparator, which includes positive feedback. Considering the switching of output voltage, *V*outfrom 1 to 0, in the case of inverter, the transition starts as soon as the input voltage reaches the threshold voltage of the PD transistor, *V*thn. On the other hand, in case of ST-based inverter, for *V*out = 1, the feedback transistor MNF is ON and the voltage at node *V*NX is *V*dd − *V*thn. In this case, the minimum voltage required at the input for switching will be much higher than *V*thn. The characteristic for inverter and ST is shown in Fig. 1(b). Due to the improved inverter characteristic, the ST-based SRAM offers higher SNM.

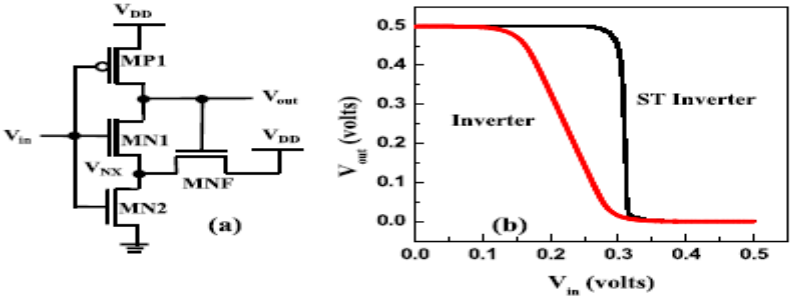

Fig.3 (a) Basic ST inverter used for this design (b) Characteristics of inverter and ST inverter for 0 →1

Previously, Kulkarni *et al.* [22] proposed ST-based differential 10T SRAM cell (hereafter referred to as ST-1) with improved RSNM and robustness. However, this cell still suffers from read–write conflict as in the conventional 6T SRAM cell. Although the RSNM is increased as compared with the conventional 6T SRAM cell due to the inherent feedback mec hanism of ST, this cell is still vulnerable to noise, since the 0 storing internal node of this cell rises to a voltage higher than ground during read operation (i.e., destructive read). Due to the voltage division between the cross-coupled ST and the access transistors, the stored data are disturbed, which is referred to as read upset [23]. An improved version of ST-based 10T SRAM cell was reported in [16] (hereafter referred to as ST-2), which uses separate signal to control the feedback transistors. It resolves the read upset problem up to higher extent as compared with ST-1 by improving the feedback mechanism. However, ST-2 includes two transistors connected to the BLs instead of one, which increases the capacitance loading (almost double as compared with ST-1) on BLs and also reduces the *I*ON/*I*OFF ratio of the read path. Larger capacitance on BLs and low *I*ON/*I*OFF ratio limit the number of cells that can share common BLs. Moreover, it takes longer time to discharge the BL during read operation, thus increasing the read-access time.

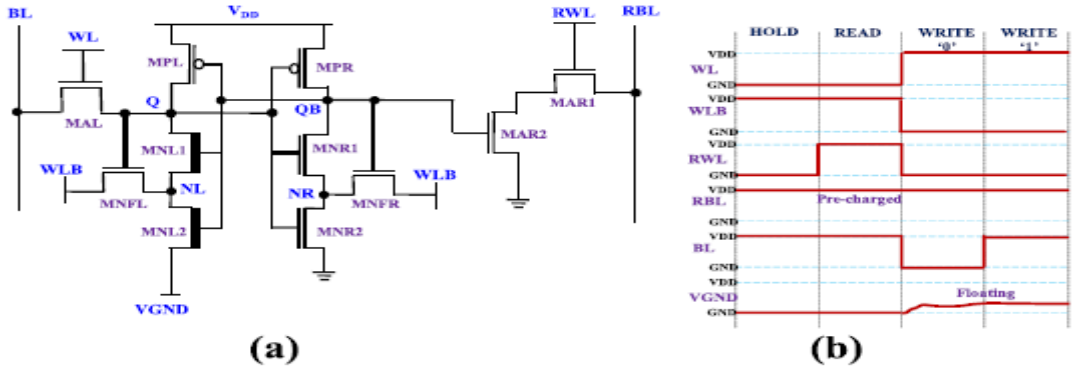

Fig.4 (a) Schematic and (b) timing diagram of control signals

Fig.4 (a) and (b) shows schematic and timing diagrams for the control signals in different modes of operation of the proposed ST11T SRAM cell. The ST11T SRAM cell consists of a cell core (cross-coupled ST inverter), a readpath consisting of two transistors, and a write-access transistor. The write-access transistor MAL is controlled by row-based WL, and the read-access transistor MAR1 is controlled by row-based read WL (RWL). The feedback transistors of ST, MNFL, and MNFR are controlled by internal storage nodes Q and QB, respectively, with their drains connected with a control signal Wordline_bar (WLB) (inverted version of write enable signal). The virtual ground (VGND) is rowbased, and WLB and BLs (BL and RBL) are column-based. If the memory is floor planned, such that all the cells of a word are adjacent to each other, then VGND signal can be easily shared over a row. However, for a bit-interleaved architecture, a hard-coding technique, as shown in Fig. 2(c), can be used to generate VGND signal for the cells of a selected word. The use of WLB and VGND control signals significantly mitigates the half-select disturb issue in the proposed cell. In the hold mode, both WL and RWL are disabled and VGND is kept grounded. Therefore, the cross-coupled ST inverter is isolated from both the BLs, and the data-holding capability is increased due to the feedback mechanism. During read operation, WL is disabled, whereas RWL is enabled, which provides discharging path for RBL through transistors MAR1 and MAR2 depending on the data stored at QB. The disabled WL makes data storage nodes (Q and QB) decoupled from BL during the read access. Due to this isolation, the RSNM is almost the same as the HSNM. Since the HSNM is very high in ST-based cell, read stability is remarkably improved. The VGND is again kept at ground, so that storage node may not get disturbed during read operation. It is to be noted that in both read and hold mode,

WLB is at *V*dd (because write enable signal is disabled), which helps the feedback transistors MNFL and MNFR to provide a feedback mechanism and to exploit the feature of ST inverter to have a good inverter characteristic. For writing data into the cell, WL is activated to transfer the data to storage node from BL, which is set/reset according to the data to be written. RWL is disabled, whereas the node VGND is kept floating. The floating VGND helps to overcome significantly write 1 problem of a single BL structure [3]. The WLB signal, which is inverted version of write enable signal, is disabled (i.e., WLB = 0 V) during the writeoperation. Consequently, there is no feedback action from any of the feedback transistors MNFL and MNFR as the voltage at nodes NL and NR does not rise. Subsequently, the writing speed is significantly increased. The proposed bitcell employs read buffers to decouple storage nodes (Q and QB) from BL to eliminate read-disturb problem along with the requirement of asymmetric write-assist mechanism for single-ended writing [3]. Therefore, there is no transistor sizing conflict for read and write operations. We could use minimum-sized devices for PD transistors, because the operation of the cell is no longer limited by the read stability problem. Decrease in the size of PD transistors reduces the leakage current along with the cell area at the expense of speed [24]. To strike a balance, we use minimum width transistors for the cell core and increase the widths of MAL, MAR1, and MAR2 by 1.5 times to reduce the access delay.

RESULTS:

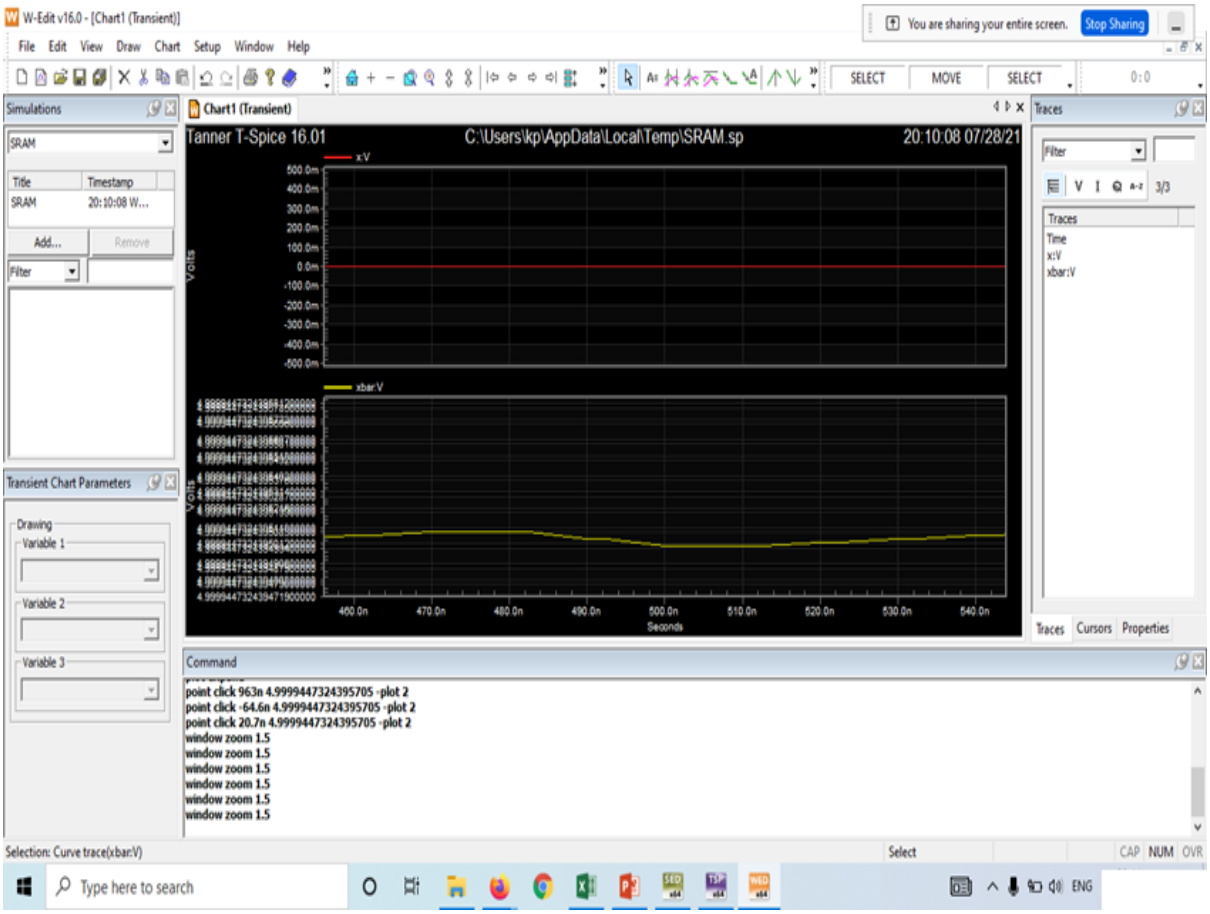

Fig: Existing simulation result

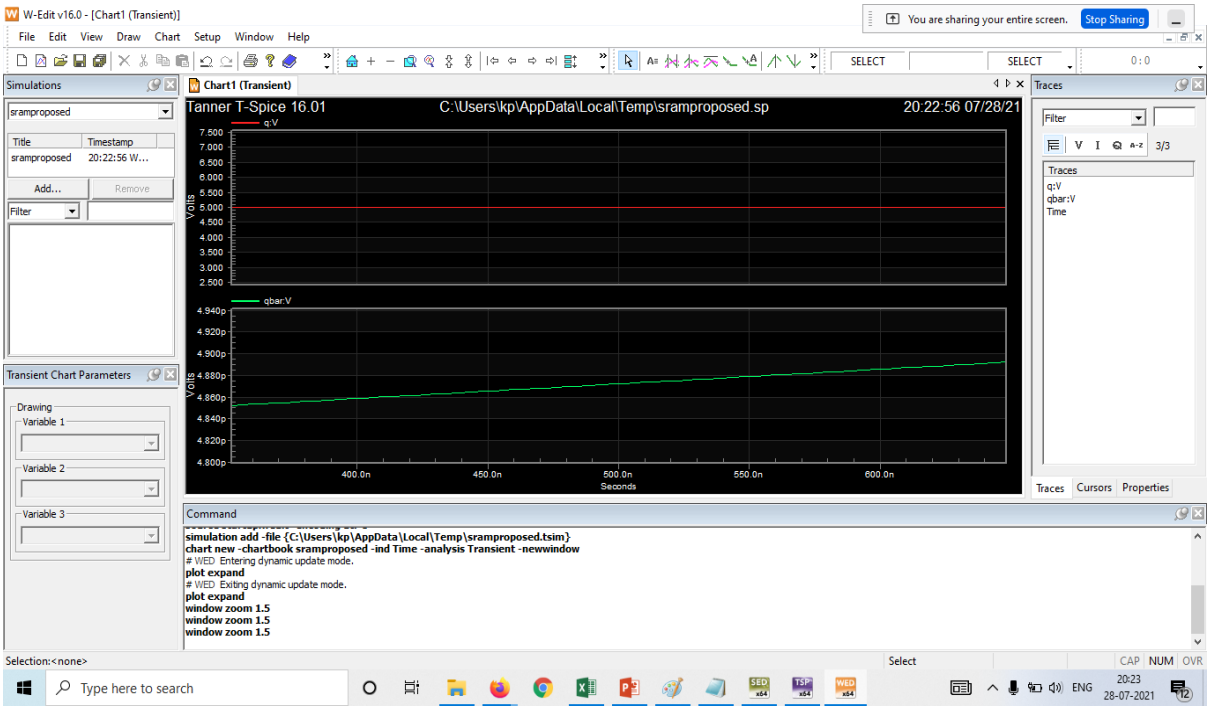

Fig: Proposed simulation result

CONCLUSION: Finally, an efficient SRAM with proposed technique is implemented, simulated and synthesized with more accurate measurement and calibrations. The different constraints variations against low power CMOS logic families are shortlisted, which shows that adiabatic logic families largely depend upon its. In this paper, we propose a test method with VDD correction for SRAM static stability test, including an addressable test structure and the corresponding test algorithm combing Bisection method and PID algorithm to correct the terminal voltages. The VDD correction is proved to be critical to accurate measurement. By using the proposed method, 1k-bits DUTs in a standard 55nm process were measured. the measurement results well match the simulation results. This validates the practicability of the method. In summary, the VDD correction is important in the test of SRAM static stability, and the proposed test method is practical for measuring SRAM static characteristics while ensuring accuracy and quantity

FUTURE SCOPE: CLOCK RATE AND POWER can be reduced by using modified architectures as follows. The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle, in the region of a few micro-watts.

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